LINEAR TECHNOLOGY

DESIGN NOTES

Safe Hot Swapping Using the LTC1421 – Design Note 139

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When a circuit board is inserted into a live backplane, the large bypass capacitors on the board can draw huge inrush currents from the backplane power bus as they charge. The inrush current, on the order of 10A to 100A, can destroy the board's bypass capacitors, metal traces or connector pins. The inrush current can also cause a glitch on the backplane power bus, which could force all of the other boards in the system to reset. In addition, the system data bus can be disrupted when the board's data pins make or break contact.

The LTC®1421 can turn on two positive and one negative board supply voltage at a programmable rate, allowing a board to be safely inserted in, or removed from, a live backplane. The chip provides internal charge pumps for driving the gates of external N-channel pass transistors, board connection sensing, flexible supply voltage monitoring, power on reset output, short-circuit protection and soft or hard reset via software control.

Typical Application

Figure 1 shows a typical application using the LTC1421.

The LTC1421 works best with a staggered, 3-level connector. Ground makes connection first to discharge any static build-up. V_{CC}, V_{DD} and V_{EE} make connection second and the data bus and all other pins last. The connection sense pins $\overline{CON1}$ and $\overline{CON2}$ are located on opposite ends of the connector to allow the board to be rocked back and forth during insertion.

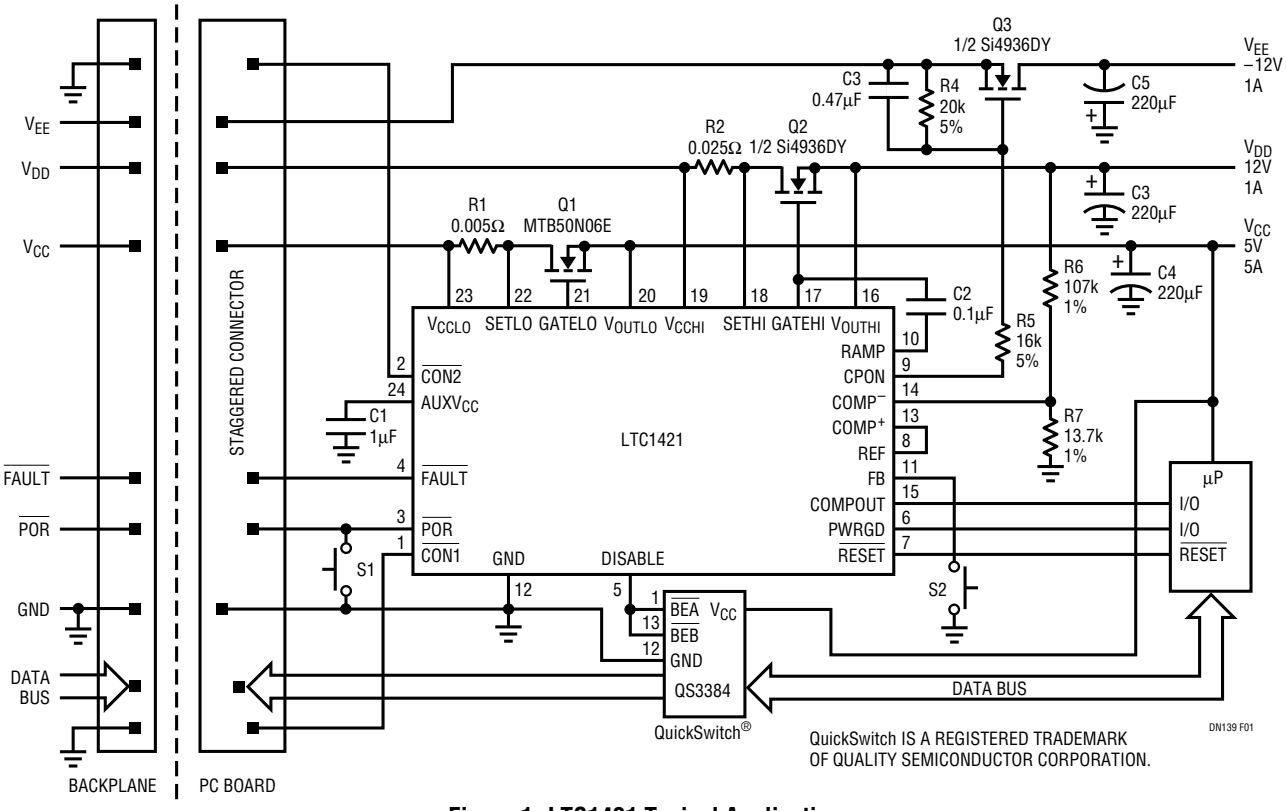

Figure 1. LTC1421 Typical Application

The power supplies on the board are controlled by placing external N-channel pass transistors Q1, Q2 and Q3 in the power path for V_{CC}, V_{DD} and V_{EE}, where V_{CC} and V_{DD} can range from 3V to 12V, and V_{EE} from –5V to –48V. By ramping up the voltage on the pass transistors' gates at a controlled rate, the transient surge current [I = (C)(dv/dt)] drawn from the main backplane supply will be limited to a safe value. The ramp rate is set by the value of capacitor C2.

The board's data bus is buffered by a QS3384 QuickSwitch from Quality Semiconductor. Disabling the QuickSwitch via the DISABLE pin during board insertion and removal prevents corruption of the system data bus.

Resistors R1 and R2 form an electronic circuit breaker function that protects against excessive supply current. When the voltage across the sense resistor is greater than 50mV for more than 20µs, the circuit breaker trips, immediately turning off Q1 and Q2 while the $\overline{FAULT}$ pin is pulled low. The chip will remain in the tripped state until the $\overline{POR}$ pin is pulsed low or the power on V_{CCLO} and V_{CCHI} is cycled. The circuit breaker can be defeated by shorting V_{CCLO} to SETLO and V_{CCHI} to SETHI.

The $\overline{RESET}$ signal is used to reset the system microcontroller. When the voltage on the V_{OUTLO} pin rises above the reset threshold, PWRGD immediately goes high and $\overline{RESET}$ goes high 200ms later. When the V_{OUTLO} supply voltage drops below the reset threshold, PWRGD immediately goes low, and $\overline{RESET}$ goes low 60µs later, allowing the PWRGD signal to be used as an early warning that a reset is about to occur. When the FB is left floating, the reset threshold is 4.65V; when the FB pin is tied to V_{OUTLO}, the reset threshold is 2.90V.

The uncommitted comparator and internal voltage reference, along with resistors R6 and R7, are used to monitor the 12V supply. When the supply drops below 10.8V, the COMPOUT pin will go low. The comparator can be used to monitor any voltage in the system.

Push-button switches S1 and S2 are used to generate a hard and soft reset, respectively. A hard or soft reset may also be initiated by a logic signal from the backplane. Pushing S1 shorts the $\overline{POR}$ pin to ground, generating a hard reset that cycles the board's power. Pass transistors Q1 to Q3 are turned off and V_{OUTLO} and V_{OUTHI} are actively pulled to ground. When V_{OUTLO} discharges to within 100mV of ground, the LTC1421 is reset and a normal power-up sequence is started.

Pushing S2 shorts the FB pin to ground, generating a soft reset that doesn't cycle the board's power. PWRGD immediately goes low, followed 64µs later by $\overline{RESET}$. When S2 is released, PWRGD immediately goes high, followed 200ms later by $\overline{RESET}$.

Board Insertion Timing

When the board is inserted, GND pin makes contact first, followed by V_{CCHI} and V_{CCLO} (Figure 2, time point 1). DISABLE is immediately pulled high, so the data bus switch is disabled. At the same time $\overline{CON1}$ and $\overline{CON2}$ make contact and are shorted to ground on the host side (time point 3). When $\overline{CON1}$ and $\overline{CON2}$ are both forced to ground for more than 20ms, the LTC1421 assumes that the board is fully connected to the host and power-up can begin. When V_{CCLO} and V_{CCHI} exceed the 2.45V undervoltage lockout threshold, the 20µA current reference is connected from RAMP to GND, the charge pumps are turned on and CPON is forced high (time point 4). V_{OUTHI} and V_{OUTLO} begin to ramp up. When V_{OUTLO} exceeds the reset threshold voltage, PWRGD will immediately be forced high (time point 5). After a 200ms delay, $\overline{RESET}$ will be pulled high and DISABLE will be pulled low, enabling the data bus (time point 6).

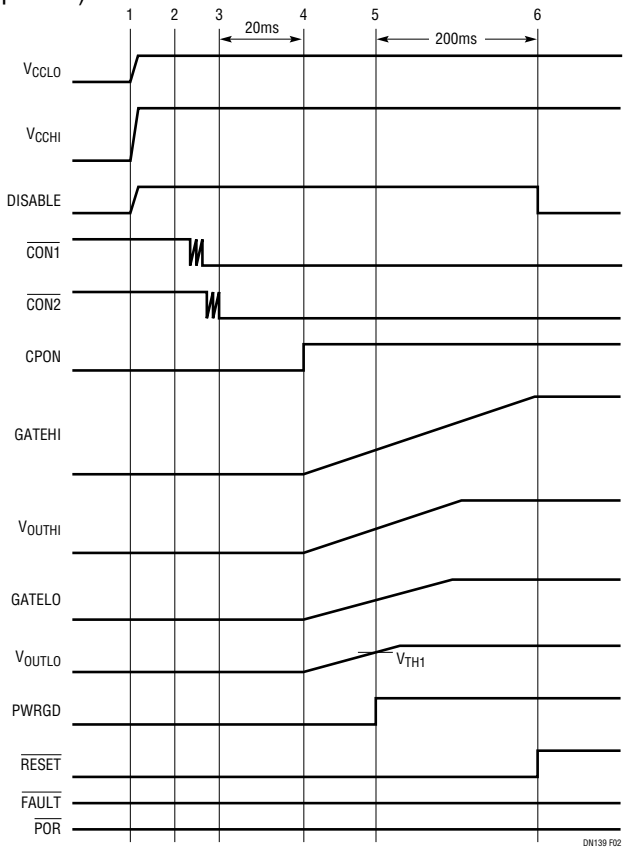

Figure 2. Board Insertion Timing

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